Verilog Test Bench Design Code

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Section 002R

CMPEN 331

Verilog Design Code

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company: Pennsylvania State University, University Park

// Engineer: Anand Rajan

//

// Create Date: 03/12/2021 11:33:07 AM

// Design Name:

// Module Name: top

// Project Name: Lab 3

// Target Devices: XC7Z010-CLG400-1

// Tool Versions:

// Description: The project aims to develop a basic CPU through pipelining.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module top(input clk, output[31:0] IM\_sig, output wreg\_sig, output m2reg\_sig, output wmem\_sig,

output[3:0] aluc\_sig, output aluimm\_sig, output[4:0] mux\_sig, output [5:0] qa\_sig,

output [5:0] qb\_sig, output [31:0] eimm\_sig);

// Block 1: IF stage

wire[7:0] adder\_to\_pc; // Output from adder

wire[7:0] pc\_out; // Output from PC register

wire[31:0] im\_to\_ifid; // Output from instruction memory

// Block 2: ID stage

wire[31:0] ifid\_out;

// Outputs from the Control Unit

wire wreg\_to\_idexe;

wire m2reg\_to\_idexe;

wire wmem\_to\_idexe;

wire[3:0] aluc\_to\_idexe;

wire aluimm\_to\_idexe;

wire RegDst;

// Output from Mux

wire [4:0]mux\_to\_idexe;

// Output from Register File

wire [5:0]qa\_to\_idexe;

wire [5:0]qb\_to\_idexe;

// Output from Sign Extender

wire[31:0] eimm\_to\_idexe;

// Block 3: EXE stage (next lab)

wire ewreg;

wire em2reg;

wire ewmem;

wire[3:0] ealuc;

wire ealuimm;

wire [4:0] emuxout;

wire [5:0] eqa;

wire [5:0] eqb;

wire [31:0] eeimm;

// Module Instantiations

PC pc(clk, adder\_to\_pc, pc\_out);

Adder adder(pc\_out, adder\_to\_pc);

IM im(pc\_out, im\_to\_ifid);

IFID ifid(clk, im\_to\_ifid, ifid\_out);

CU cu(ifid\_out[31:26], ifid\_out[5:0], wreg\_to\_idexe, m2reg\_to\_idexe, wmem\_to\_idexe, aluc\_to\_idexe, aluimm\_to\_idexe, RegDst);

Mux mux(ifid\_out[15:11], ifid\_out[20:16], RegDst, mux\_to\_idexe);

Regfile regfile(ifid\_out[25:21], ifid\_out[20:16], qa\_to\_idexe, qb\_to\_idexe);

Signext ext(ifid\_out[15:0], eimm\_to\_idexe);

IDEXE idexe(clk, wreg\_to\_idexe, m2reg\_to\_idexe, wmem\_to\_idexe, aluc\_to\_idexe,

aluimm\_to\_idexe, mux\_to\_idexe, qa\_to\_idexe, qb\_to\_idexe, eimm\_to\_idexe,

ewreg, em2reg, ewmem, ealuc, ealuimm, emuxout, eqa, eqb, eeimm);

// Since the instructions ask for signals written INTO each register and not from, the following are outputs:

assign IM\_sig = im\_to\_ifid;

assign wreg\_sig = wreg\_to\_idexe;

assign m2reg\_sig = m2reg\_to\_idexe;

assign wmem\_sig = wmem\_to\_idexe;

assign aluc\_sig = aluc\_to\_idexe;

assign aluimm\_sig = aluimm\_to\_idexe;

assign mux\_sig = mux\_to\_idexe;

assign qa\_sig = qa\_to\_idexe;

assign qb\_sig = qb\_to\_idexe;

assign eimm\_sig = eimm\_to\_idexe;

endmodule

module PC(input clk, input[7:0] a, output reg[7:0] q);

// Wire to set the value of PC to its next value; PC is a register effectively

always @(posedge clk)

begin

q <= a;

end

initial begin

q = 8'd100;

end

endmodule

module Adder(input [7:0]a, output reg[7:0] q);

// This module is not clock-dependent. It adds the input from PC register to the constant 4 and returns it.

// PC register should take this value to set as new value.

wire[7:0] to\_add = 8'd4;

always @(\*)

begin

q <= (a + to\_add);

end

endmodule

module IM(input[7:0] addr, output reg [31:0] do);

reg [31:0] IM [0:511]; // Array of registers

integer a;

always @(\*)

begin

a = addr; // integer-cast

do = IM[a];

end

initial // Hardcoded based on the examples provided to be done

begin

IM[100] = 32'b10001100001000100000000000000000;

IM[104] = 32'b10001100001000110000000000000100;

end

endmodule

module IFID(input clk, input [31:0]a, output reg[31:0] q);

// This is also clock-dependent. Outputs whatever it's inputted at pos clock edge.

always @(posedge clk)

begin

q <= a;

end

endmodule

module CU(input [5:0] op, input [5:0] func,

output reg wreg, output reg m2reg, output reg wmem, output reg[3:0] aluc, output reg aluimm, output reg regrt);

always @(\*) begin

case(op) // Determination of these values depends on the opcode, and func for R-format

6'b000000: // R-format instruction

begin

wreg = 1'b1;

m2reg = 1'b0;

wmem = 1'b0;

regrt = 1'b1;

aluimm = 1'b0;

case(func) // Using truth table in Zybooks

6'b100000: // add

aluc = 4'b0010;

6'b100010: // subtract

aluc = 4'b0110;

6'b100100: // AND

aluc = 4'b0000;

6'b100101: // OR

aluc = 4'b0001;

6'b100110: // XOR

aluc = 4'b0010;

6'b000000: // shift left

aluc = 4'b0010;

6'b000010: // logical shift right

aluc = 4'b0110;

// Not in truth table

// 6'b000011: // arithmetic shift right

// aluc = 4'b0010;

// 6'b001000: // register jump

// aluc = 4'b0010;

endcase

end

// Commented cases remain to be done in second part of lab - only necessary cases done

// 6'b001000: // addi

// 6'b001100: // andi

// 6'b001101: // ori

// 6'b001110: // xori

6'b100011: // lw

begin

wreg = 1'b1;

m2reg = 1'b1;

wmem = 1'b0;

regrt = 1'b0;

aluimm = 1'b1;

aluc = 4'b0010;

end

6'b101011: // sw

begin

wreg = 1'b0;

m2reg = 1'bX;

wmem = 1'b1;

regrt = 1'bX;

aluimm = 1'b1;

aluc = 4'b0010;

end

// 6'b000100: // beq

// 6'b000101: // bne

// 6'b001111: // lui

// 6'b000010: // j

// 6'b000011: // jal

endcase

end

endmodule

module Mux(input [4:0]rd, input [4:0]rt, input regrt, output reg [4:0]muxout);

always @(\*) begin

if (regrt) // select rd if RegDst is 1

muxout <= rd;

else // select rt if RegDst is 0

muxout <= rt;

end

endmodule

module Regfile(input [4:0]rs, input [4:0]rt, output reg [5:0]qa, output reg [5:0]qb);

reg [31:0] regfile [0:31];

integer a;

integer b;

always @(\*) begin

// qa outputs for rs and qb outputs for rt

a = rs; // this is to integer-cast the binary input

b = rt;

qa <= regfile[a];

qb <= regfile[b];

end

// asked to initialize all values in the regfile to 0

integer i;

initial begin

for (i=0; i<32; i=i+1) begin

regfile[i] = 0;

end

end

endmodule

module Signext(input [15:0]imm, output reg [31:0]eimm);

// converts 16 bit imm to 32 bits

always @(\*) begin

eimm[31:0] <= { {16{imm[15]}}, imm[15:0] };

end

endmodule

module IDEXE(input clk, input wreg, input m2reg, input wmem, input [3:0]aluc, input aluimm, input [4:0]muxout, input [5:0]qa, input [5:0]qb, input [31:0]eimm,

output reg ewreg, output reg em2reg, output reg ewmem, output reg [3:0]ealuc, output reg ealuimm, output reg [4:0]emuxout,

output reg [5:0]eqa, output reg [5:0]eqb, output reg[31:0] eeimm);

// Nothing but a clock-dependent output-input setter

always @(posedge clk)

begin

ewreg <= wreg;

em2reg <= m2reg;

ewmem <= wmem;

ealuc <= aluc;

ealuimm <= aluimm;

emuxout <= muxout;

eqa <= qa;

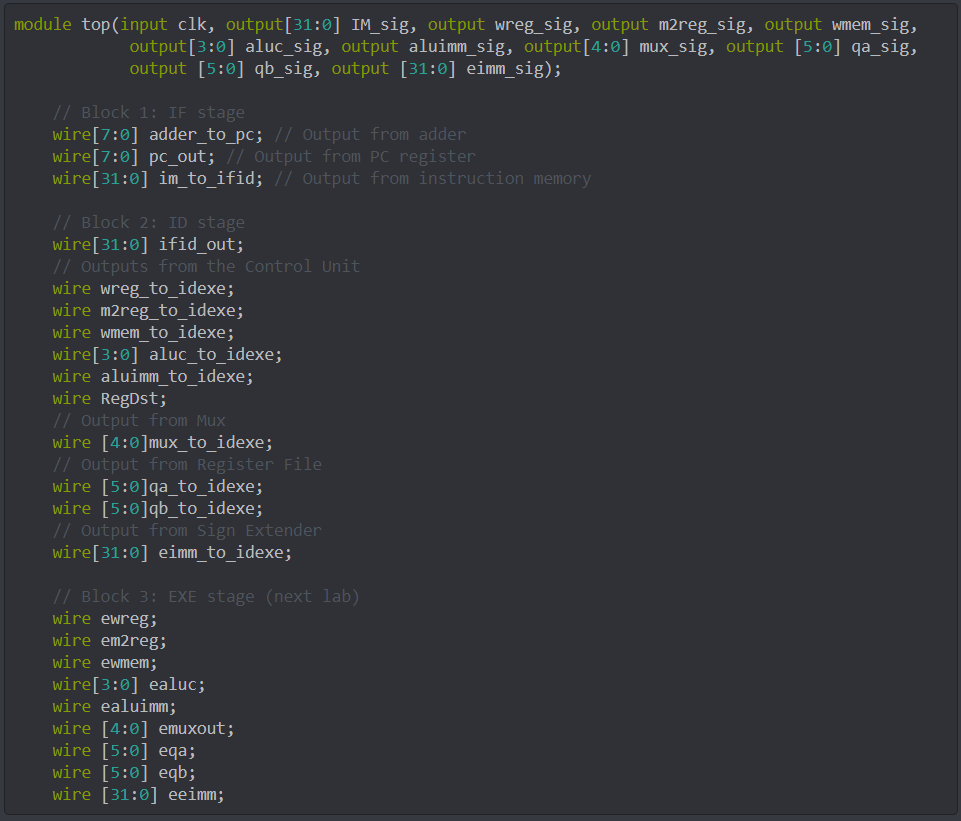
eqb <= qb;

eeimm <= eimm;

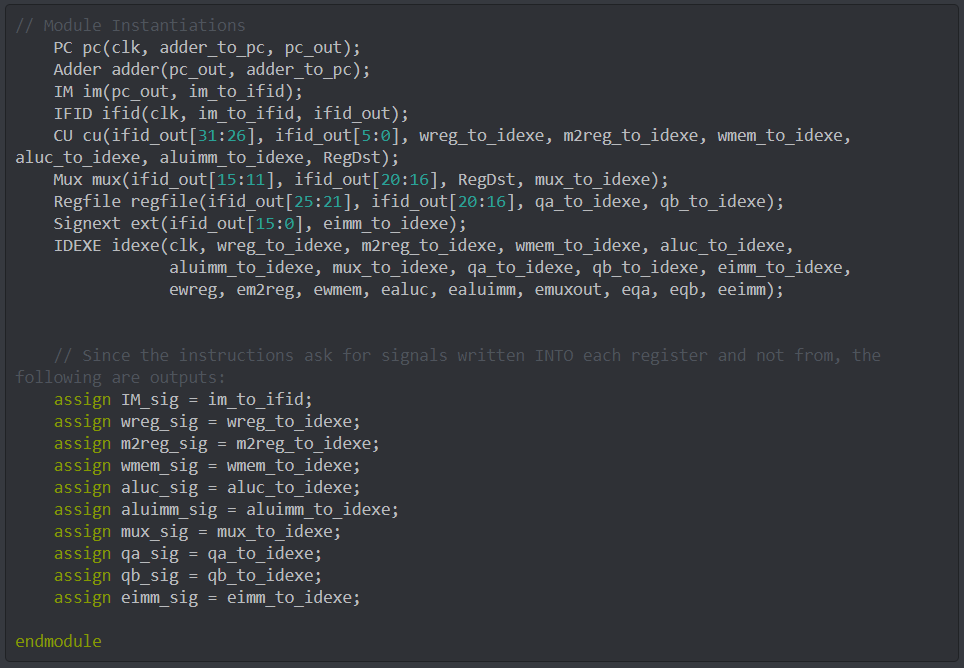
end

endmodule

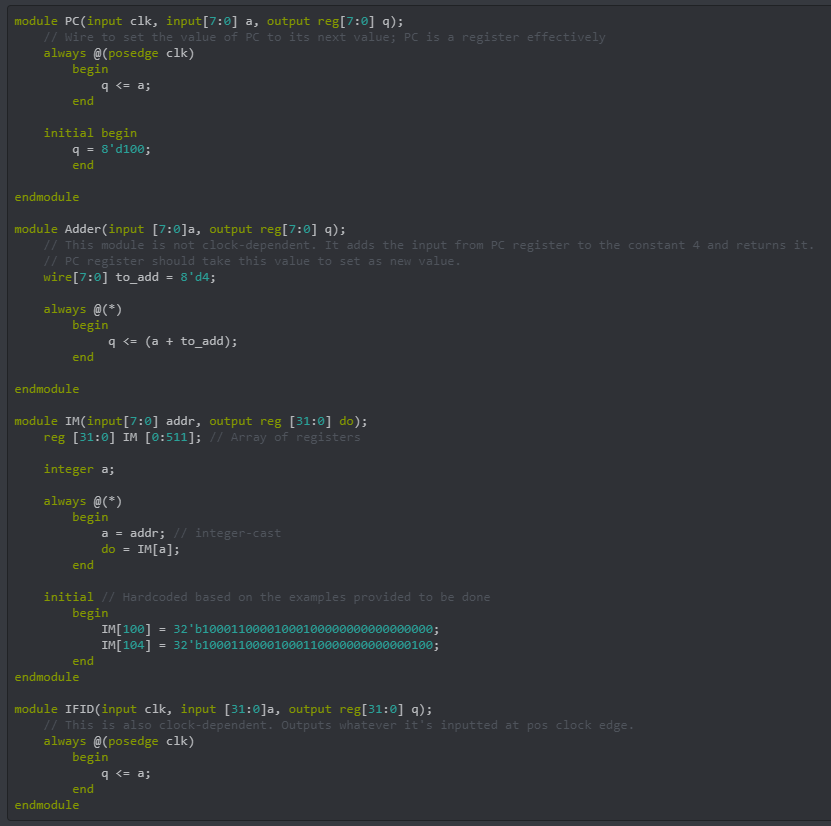
Note that the device used, as listed in the prefacing comments, is XC7Z010-1CLG400-1, as prescribed by the laboratory instructions. For readability purposes, screenshots of the same code are provided with keyword color highlighting as well as indentation displayed below (with the omission of the prefacing comments). The provision of the testbench code as well as screenshots of the same will follow this section.



*Image 1. Screenshot containing first section of Verilog design code – included for display, readability, and aesthetic purposes.*



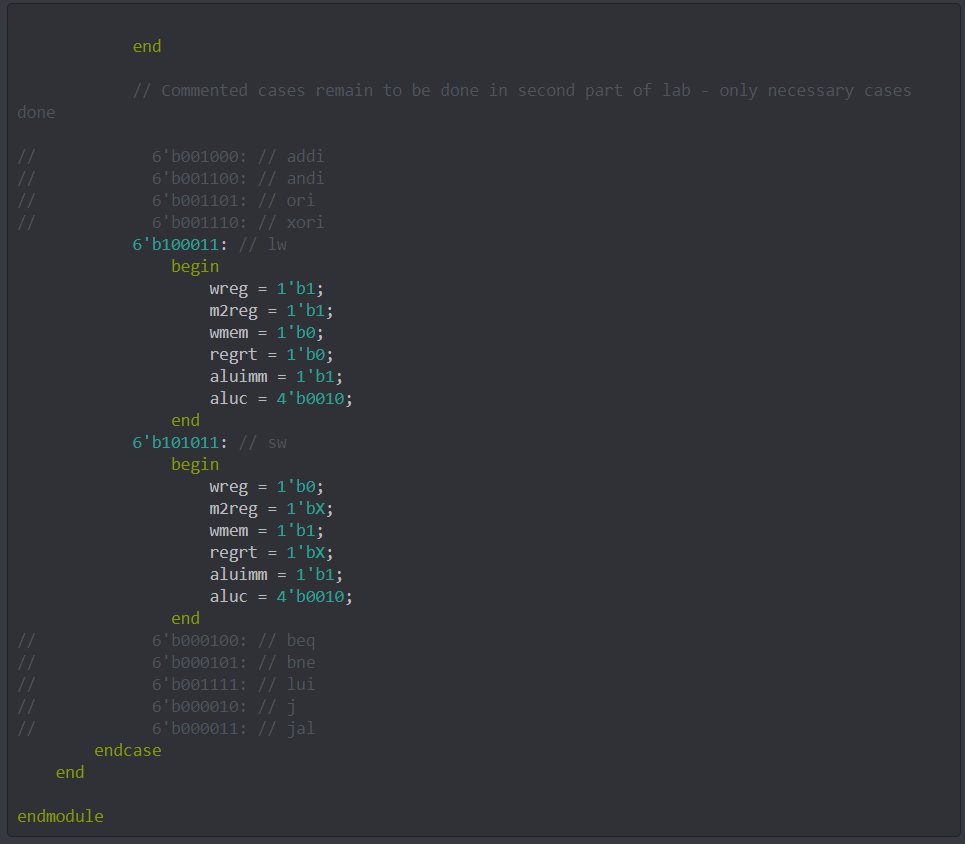
*Image 2. Screenshot containing second section of Verilog design code – included for display, readability, and aesthetic purposes.*



*Image 3. Screenshot containing third section of Verilog design code – included for display, readability, and aesthetic purposes.*



*Image 4. Screenshot containing fourth section of Verilog design code – included for display, readability, and aesthetic purposes.*



*Image 5. Screenshot containing fifth section of Verilog design code – included for display, readability, and aesthetic purposes.*



*Image 6. Screenshot containing fifth and final section of Verilog design code – included for display, readability, and aesthetic purposes.*

Verilog Test Bench Design Code

//////////////////////////////////////////////////////////////////////////////////

// Company: Pennsylvania State University, University Park

// Engineer: Anand Rajan

//

// Create Date: 03/14/2021 10:04:14 PM

// Design Name: Pipelining CPU

// Module Name: top

// Project Name: Lab 3

// Target Devices: XC7Z010-CLG400-1

// Tool Versions:

// Description: The project aims to develop a basic CPU through pipelining.

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

`timescale 1ns/1ps

module testbench();

reg clk\_tb = 0;

wire[31:0] IM\_sig;

wire wreg\_sig;

wire m2reg\_sig;

wire wmem\_sig;

wire[3:0] aluc\_sig;

wire aluimm\_sig;

wire[4:0] mux\_sig;

wire [5:0] qa\_sig;

wire [5:0] qb\_sig;

wire [31:0] eimm\_sig;

top dut(clk\_tb, IM\_sig, wreg\_sig, m2reg\_sig, wmem\_sig, aluc\_sig, aluimm\_sig, mux\_sig, qa\_sig, qb\_sig, eimm\_sig); // Initializing an instance of top

always begin

#5;

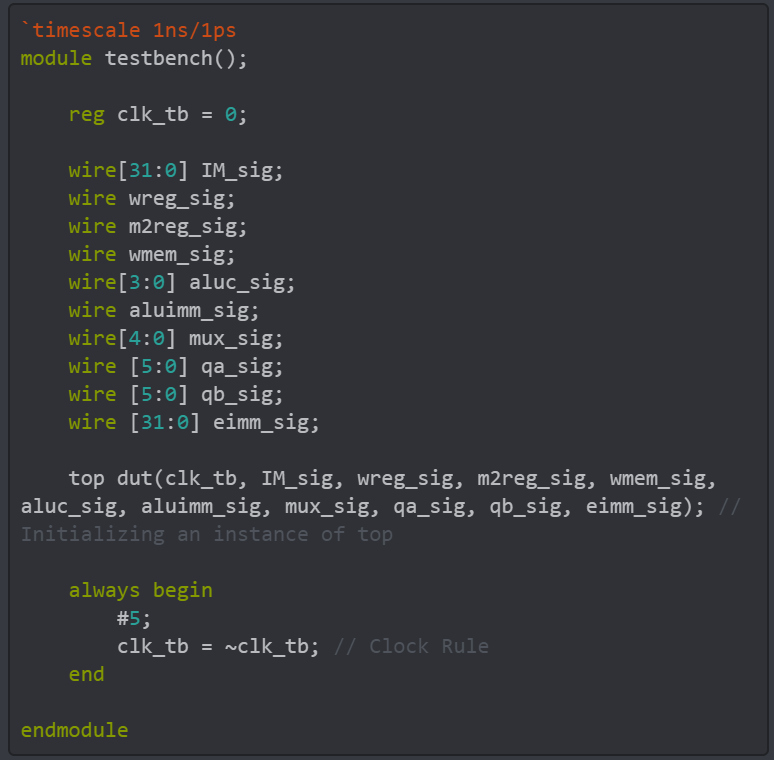
clk\_tb = ~clk\_tb; // Clock Rule

end

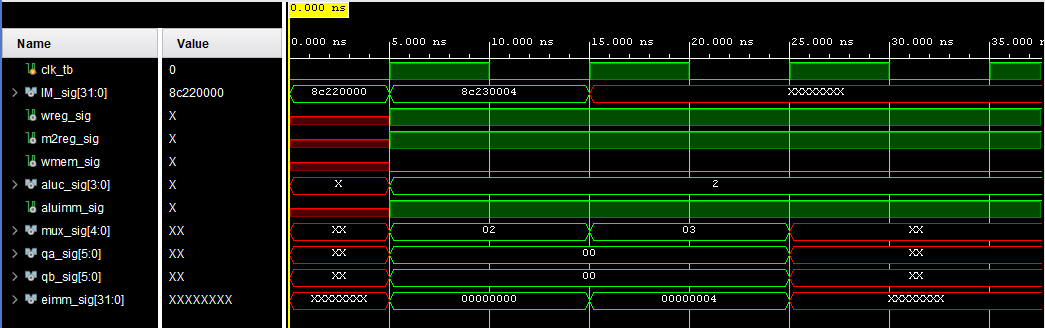
endmodule

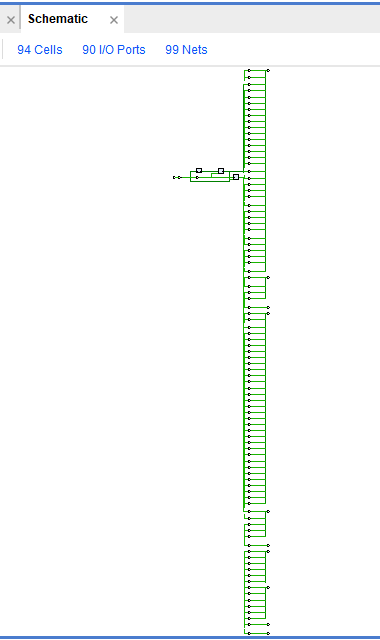
Note that this function really only requires the controlling of the clock through the testbench. These outputs are displayed as outputs for simplicity but the $display keyword could also have been used in place of this. Once again, for readability purposes, screenshots of the same code is provided with keyword color highlighting as well as indentation displayed below (with the omission of the prefacing comments).

The corresponding waveforms for the simulation of this design and testbench design code is also provided below the code screenshot. It should be stressed that the signals become X once more after 25 ns due to the lack of instructions past the PC’s of 100 and 104. Since most of these blocks perform calculations or selections, there is no selection to be made if there is no instruction derived from the IM. As such, they are X’s. The signals that come as outputs from the Control Unit extend forever PURELY BECAUSE OF THE CASE STATEMENT. No default statement was introduced since no such case was presented to account for this, and as such, with the lack of instructions, the control unit continues to output the same values as before infinitely. **THIS IS NOT A BUG. THIS CAN BE CHANGED WITH MORE INSTRUCTIONS OR SPECIFICATION OF A DEFAULT CASE.** All values for each signal are found on the signal and not on the left-hand sidebar. Refer to the signals themselves (those without values are logic signals).

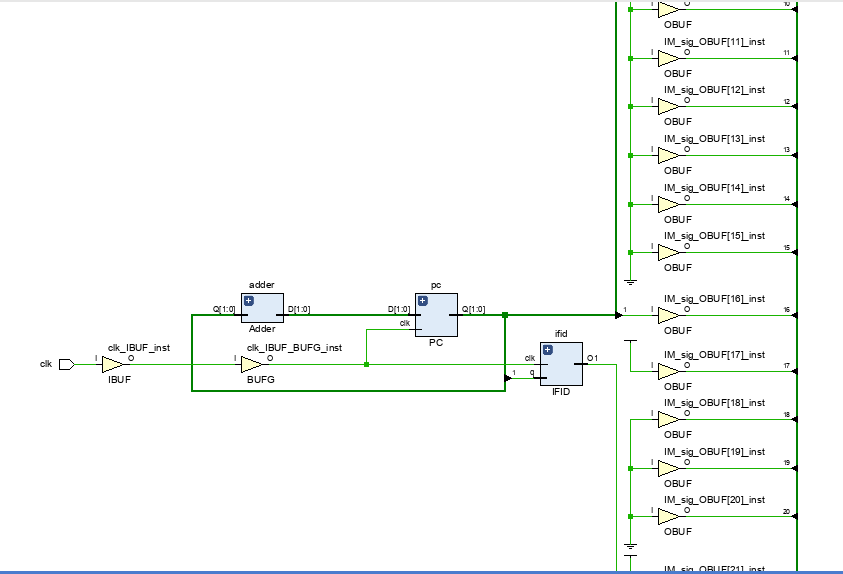


*Image 7. Screenshot of Verilog Test Bench Design Code provided for readability and aesthetic purposes*

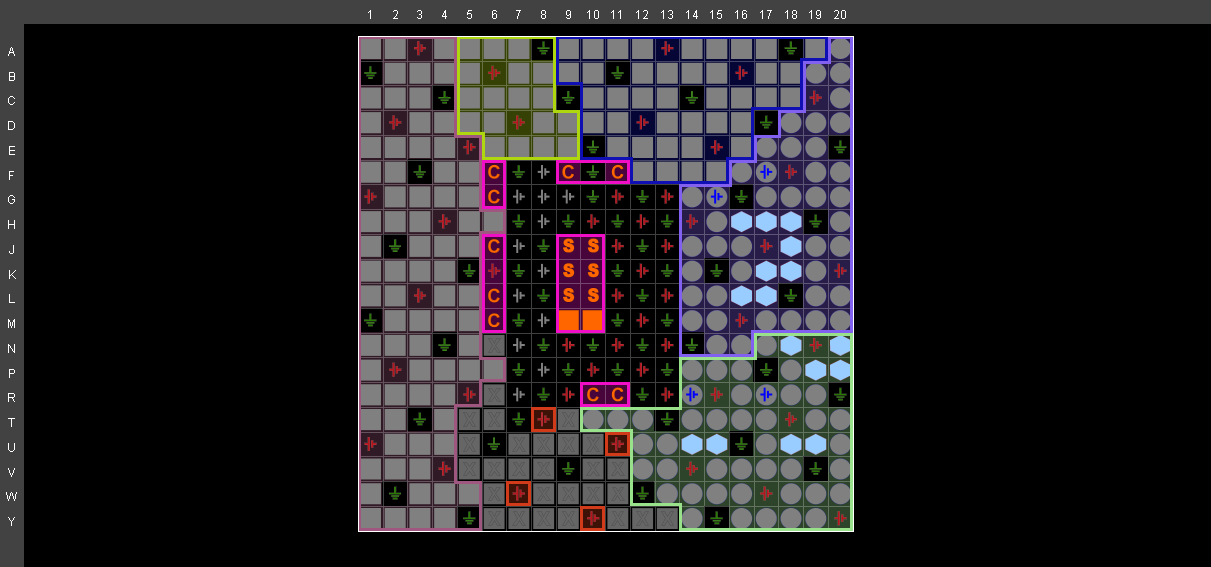
  
*Image 8. Screenshot of Final Waveform*



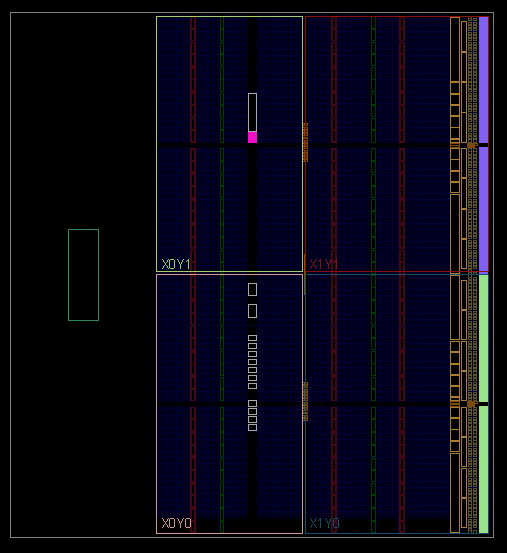
*Image 9. Design Schematics from the Synthesis of the Project (****SYNTHESIZED DESIGN –*** *xc7z010clg400-1)*



*Image 10. A close-up of what zooming into the center yields. Everything could not be zoomed in on for space’s sake.*



*Image 11. Snapshot of the I/O Planning*



*Image 12. Snapshot of the Floor Planning*

Images 14 through 16 provide the design schematic of the synthesized design and snapshots of the I/O and Floor planning of the same. It was difficult to discern which was which due to GUI errors, so the same choices of images were taken as the first lab. Note that the schematic provided could not be zoomed or resized in any way to make it clearer or larger. The information of the schematic is provided just above the design, in the same bar where the number of cells and such are mentioned. Specifics can be conducted within the project itself. The vertical layout was indeterminable though, and as such, cannot be zoomed in on without cutting a large portion out (or without having to post 20 or so snapshots).

With this, the requirements specified by the lab’s instructions are concluded. To recap, the specified device was used in this lab, which was done in Vivado. The Verilog design code as well as test bench code were both provided (albeit not with the 2x line spacing condition in both cases, but with 1x in the larger one in order to fit the code into as compact a space as possible – which still ended up being large). The code accounted for the blocks 1 and 2 of the basic CPU requested. Snapshots of the same were also provided in order to supplement readability and aesthetics such as indentations and comments. The waveform resulting from the verification of my design using the simulation software were also provided, with all the specified signals shown. The waveforms cover a timing period from 0 till 25 ns, since this is all the time necessary for 2-3 clock cycles (by which time the instructions will have come to pass). Additionally, the design was synthesized and the design schematics of this as well as the I/O and Floor planning designs were provided in snapshots (images 14 through 16). The cover page requirements were met to the best of my ability, and this project will be uploaded as a Word file (with no use of LaTex).